## REMARKS

In the last Office Action, the Examiner withdrew the previously noted allowability of claims 2-5. The Examiner also objected to claims 3-5 and 8-12 as containing informalities and rejected claims 1, 3-5 and 7-12 under 35 U.S.C. §103(a) over a new combination of the references to APD (applicant's prior art disclosure in Fig. 2) and Kocon (USPN 6,351,009).

In accordance with the present response, independent claims 1 and 7 have been amended to further patentably distinguish from the combination of APD and Kocon by changing "an insulator" to "side spacers." This amendment is supported by the disclosure of the embodiment of the vertical MOS transistor shown in Fig. 12 and described on page 15 of the specification (lines 6-23) in which side spacers 12 are formed on side walls of the trench 4 above the heavily doped polycrystalline silicon gate 6. Claims 3 and 11 have also been amended to conform to the proposed amendments to claims 1 and 7, respectively. New claims 13-24 have been added to provide a fuller scope of coverage.

Applicant requests reconsideration of his application in light of the foregoing amendments and the following discussion.

## Objection to Claims 3-5 and 8-12

The Examiner objected to claims 3-5 and 8-12 as containing informalities because in the preamble of each claim the article "A" should be "The" and the semicolon should be a comma. Applicants respectfully traverse the Examiner's objection.

The use of the article "A" instead of "The" to preface the preamble of the dependent claims and the use of a semicolon instead of a comma to separate the preamble from the body of the dependent claims are standard and widely accepted claim drafting techniques. The Examiner's attention is directed to U.S. Patent Nos. 7,056,836 and 6,995,055, for example, which include claims using such claim drafting techniques.

In view of the foregoing, applicant respectfully requests that the objection to claims 3-5 and 8-12 be withdrawn.

## Summary of the Invention

The present invention relates to a semiconductor device. With reference to the embodiment shown in Fig. 12, amended independent claim 1 requires a semiconductor substrate 1 of a first conductivity type, an epitaxial growth layer 2 of the first conductivity type formed on the semiconductor

substrate 1, a body region 3 of a second conductivity type formed on the epitaxial growth layer 2, a heavily doped body contact region 8 of the second conductivity type formed on a part of a surface of the body region 3, and a heavily doped source region 7 of the first conductivity type formed on a part of the surface of the body region 3 that is not covered with the heavily doped body contact region. A silicon trench 4 pierces the body region 3 and the heavily doped source region 7 to reach an inner part of the epitaxial growth layer 2. A gate insulating film 5 is formed along side wall surfaces and bottom surfaces of the silicon trench 4. A heavily doped polycrystalline silicon gate 6 is buried in the silicon trench 4 over the gate insulating film 5 to a level of the heavily doped source region 7. An intermediate insulating film 9 is formed on the heavily doped polycrystalline silicon gate 6 in the silicon trench 4 to reach a surface of the semiconductor substrate 1. Side spacers 18 are disposed on the side walls of the silicon trench 4 and above the heavily doped polycrystalline silicon gate 6. A metallic source electrode 15 having a flat surface is disposed in contact with the intermediate insulating film 9, the heavily doped source region 7, and the heavily doped body contact region 8. A metallic drain electrode 16 is connected to a rear surface of the semiconductor substrate 1.

By the foregoing construction, the vertical MOS transistor according to the present invention has a higher drive performance, reliability and yield as compared to the conventional art described on pages 1-4 of the specification. The vertical MOS transistor of the present invention also has a reduced size and is economical to manufacture as compared to the conventional art.

**Traversal of Prior Art Rejection**

Claims 1, 3-5 and 7-12 were rejected under 35 U.S.C. §103(a) as being unpatentable over APD in view of Kocon. Applicant respectfully traverses this rejection and submits that the combined teachings of APD and Kocon do not disclose or suggest the subject matter recited in amended independent claims 1 and 7 and dependent claims 3-5 and 8-12.

Each of independent claims 1 and 7 has been amended to recite side spacers disposed on the side walls of the silicon trench and above the heavily doped polycrystalline silicon gate. This amendment is supported, for example, by the disclosure of the embodiment of the vertical MOS transistor shown in Fig. 12 and described on page 15 of the specification (lines 6-23) in which side spacers 12 are formed on side walls of the trench 4 above the heavily doped polycrystalline silicon gate 6. No corresponding structure is disclosed or suggested by the combined teachings of APD and Kocon.

As recognized by the Examiner, APD does not disclose or suggest any structure corresponding to side spacers disposed on the side walls of the silicon trench and above the heavily doped polycrystalline silicon gate, as recited in amended claims 1 and 7.

The secondary reference to Kocon does not cure the deficiencies of APD. More specifically, in the trench MOS-gated device shown in Fig. 2B of Kocon, a dielectric layer 212 corresponds to the intermediate insulating film recited in claims 1 and 7. Other than the dielectric layer 212, Kocon does not disclose any other structure that is formed on the sidewalls 208 of the trench 207 and, particularly does not disclose side spacers formed on the side walls of the trench above the silicon gate, as recited in amended claims 1 and 7. Accordingly, one of ordinary skill in the art would not have been led to modify the references to attain the claimed subject matter.

Claims 3-5 and 8-12 depend on and contain all of the limitations of amended independent claims 1 and 7, respectively, and, therefore, distinguish from the combined teachings of APD and Kocon at least in the same manner as claims 1 and 7.

In view of the foregoing, applicant respectfully request that the rejection of claims 1, 3-5 and 7-12 under 35 U.S.C. §103(a) as being unpatentable over APD in view of Kocon be withdrawn.

Applicant respectfully submits that the prior art of record also does not disclose or suggest the subject matter recited in newly added claims 13-24.

New claims 13-16 and 17-20 depend on amended independent claims 1 and 7, respectively, and, therefore distinguish from the combined teachings of APD and Kocon at least in the same manner as claims 1 and 7.

Moreover, new claims 13-16 and 17-20 are separately patentable from the combined teachings of APD and Kocon.

New claims 13 and 17 include the additional limitation that the intermediate insulating film is formed directly on the heavily doped polycrystalline silicon gate and the side spacers. No corresponding structure is disclosed or suggested by the prior art of record. For example, APD and Kocon do not disclose the side spacers recited in amended claims 1 and 7, and the insulating film in each of these references is formed directly on sidewalls of the transistor trench.

Claims 14-16 and 18-20 are directed to the specific positional relationship between the side spacers, the gate insulating film and the intermediate insulating film (claims 14, 18), the side spacers and the intermediate insulating film being made of different materials (claims 15, 19), and the side spacers being separate and independent from the gate insulating film and the intermediate insulating film (claims 16, 20). Again, no corresponding structure is disclosed or suggested by the prior art of record.

New independent claim 21 is directed to a vertical MOS transistor. The combined teachings of APD and Kocon do not disclose or suggest a vertical MOS transistor having an insulator separate and independent from the gate insulating film and the intermediate insulating film and disposed on the side walls of the silicon trench and above the heavily doped polycrystalline silicon gate, as recited in claim 21. In Kocon, for example, while portions of the dielectric layer 212 (intermediate insulating film) may be interpreted by the Examiner as corresponding to the "insulator" recited in claim 21, such portions correspond to unitary parts of the dielectric layer 212 and are therefore not separate and independent from the dielectric layer 212.

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New claims 22-24 depend on claim 21 and are directed to various features of the preferred embodiment which are not disclosed or suggested by the prior art of record.

In view of the foregoing amendments and discussion, the application is believed to be in allowable form. Accordingly, favorable reconsideration and allowance of the claims are most respectfully requested.

Respectfully submitted,

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**MAILING CERTIFICATE**

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AUGUST 16, 2006
Date